RECYCLING OF BROKEN SI BASED STRUCTURES AND SOLAR CELLS

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ABSTRACT: This paper presents works where broken solar cell structures early in the PV production process chain as well as broken finished solar cells have been recycled into new Si feedstock through demetallization step, purification and directional solidification. The paper discuss two different routes for removal of diffusion layers and anti-reflection coating (ARC). It also presents characterizations of ingots produced with the Si-feedstock from the two routes by directional solidification.

1 INTRODUCTION

The CABRISS project is a European collaboration between 16 partners from 9 countries; 6 SMEs, 5 Industry and 5 RTO (Research Organization) [1]. The main vision of the project is to develop a circular economy mainly for the photovoltaic, but also for other industries such as electronic or metallurgy. It will consist in the implementation of recycling technologies to recover In, Ag and Si for the sustainable PV technology and others applications.

At the moment, there is few quantity available of end-of-life modules and processes for dismantling are not fully operate, e.g. recovery of cells from the encapsulates is at lab-scale level. On the other hand, broken cells and wafers are available even at little quantity (1 to 3% of the production) due to a combination of rough handling and mechanical weaknesses in PV-material. Until now, these cells have been considered to be waste and not valuable enough for recycling.

The paper investigates two routes for the removal of ARC and diffusion layers on broken cells either coming from the cell manufacturing or from end of life module. One route use etching of ARC and diffusion layer before melting and directional solidification whereas the other route use melting, vacuum treatment and subsequent directional solidification.

The results of this study can be transferred to cells from end-of-life modules.

2 EXPERIMENTAL SETUP

This section describes the two routes for removal of ARC and diffusion layers. The first route was explored at SINTEF in Trondheim, Norway at Lab scale, and at FEROANTALTICA (FAID) at larger scale, whereas the second route was tested at CEA-INES.

2.1 Input materials

LOSER Chemie, one of the partner of CABRISS, is able to remove and recover the aluminium rear contact and the silver and indium from broken solar cells [2,3]. The solar cell scraps provided by LOSER Chemie are shown in Figure 1.

Figure 1: Broken solar cell pieces (Si-shards) delivered from LOSER Chemie. The front finger and Al back contacts have been removed. The size of pieces are about 2 - 20 mm. (courtesy LOSER Chemie GmbH).

By use of a fresh solution of aluminium chloride and water, LOSER Chemie has developed a procedure to remove the aluminium from the back side of Si solar cell and simultaneous recover a valuable product. During the reaction, [Aln(OH)mCl3n-m] (poly-aluminium-hydroxide-chloride) is formed which is usually produced by pressure digestions of aluminium hydroxide and concentrated hydrochloric acid at high temperatures.

LOSER's hydrometallurgical extraction for the recycling of silver from waste silicon cells operates at room temperature and the used alkane sulfonic acid is readily biodegradable (OECD 301 A). The alkane sulfonic acid is used as a transport system, and can be recovered.

The process runs without formation of nitrous gases, as they normally will, with use of nitric acid in the field of silver recovering. The recovery of the silver using sulfonic acids is a novel and the most effective, economical and ecologically method. A major advantage is particularly the extremely high solubility of silver salts of the corresponding sulfonic acids.

After the aluminium back and silver front contacts has been removed, the ARC layer and a front (P) and back (Al) doping field still remains and has to be removed before the

shards can be used as in a conventional melting and directional solidification step.

Figure 2 shows Tof-SIMS analysis of the back layer of a cell piece from LOSER. It is clear that aluminium has a diffused thickness about 10µm into the bulk silicon from the rear contact.

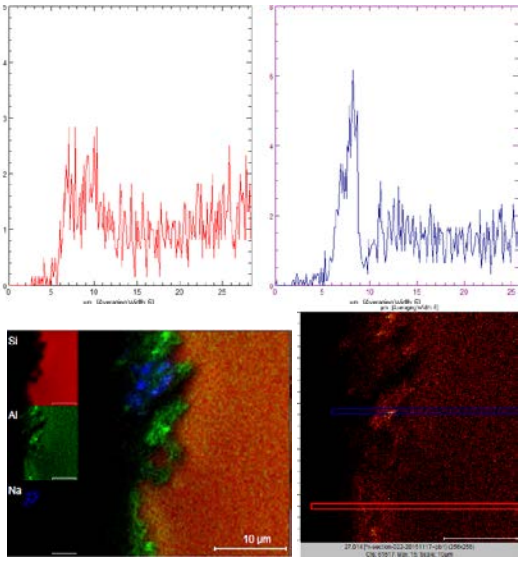


Figure 2: Tof-SIMS analysis of the back side of Si solar cell structure after removal of front and back side contacts. The upper graphs are two line scans for aluminium along the lines in lower right picture.

The other type of material tested was broken wafers from an early stage in the cell processing line at SOLITEK. These cells were taken out after PECVD and contain phosphorus diffusion layer and ARC (Si_3N_4 anti-reflection coating) in front, but no aluminium diffusion layer at the back. The thickness of these front layers are considered to be about 1µm.

It is clear that from the layer thickness measurements, the LOSER-material should have a thickness reduction of about 20µm (we are not able to etch 10µm from the back side only), and the SOLITEK material would require only 2µm to be removed [4, 5].

2.2 Etching procedure

Four different etching techniques have been tested in small scale and a method for larger batches were developed for two of the etching technique tested. The challenge was to choose an etching solution with fast enough reaction, environmental friendly, and yet not too violent (exothermic), to be suitable for etching away the layers in relatively large batches. First small scale experiments (1 liter acid + 65 g Si scrap) were done to verify if a composition of acids was suitable. If suitable, an upscaling to 5 liters acid and 600 g Si scrap was done. The composition of the four etching techniques are shown in Table 1.

[1] The "Used polish etch" has been used to do chemical polishing of other silicon samples previously.

Table 1: Composition of the four etches that were tested.

Content	Used polish etch	CP4	"Alexander's etch"	Used and new 9:1 etch
HNO_3 (65%)	3	5	4.6	9
HF (50%)	1	3	1.5	1
CH_3COOH	3	3		
H_3PO_4 (85%)			1.5	
DI-water			2.3	

A schematic of the etching set-up experiments is shown in Figure 3.

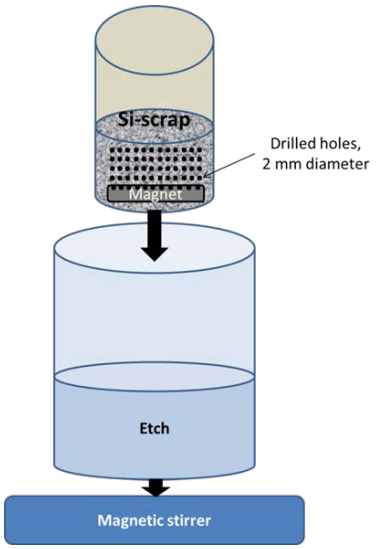


Figure 3: Principle sketch of the setup used for the small scale experiments at SINTEF (not to scale).

All four etch types were tested in small scale. The chemical reaction with the use of "Used polish etch"[1] and the "9:1" etch were reaction was gentle with little heat generation. The other two etches were considered too fast and violent.

After deciding the etch type, the setup was upscaled to 600g batches and in total 12 kg scrap was etched for use in the Crystallox DS250 furnace at SINTEF. According to thickness measurements done during the etching, about 20 – 30µm was removed from both sides of the flakes. This should be good enough for removal of both front and back layers.

2.3 Vacuum treatment process

An alternative route to remove emitter and layers is by vacuum treatment, as proposed by CEA-INES. In the case of p-type cells technology, diffusion layer contain high phosphorous concentration. As it shown on Figure 4, vapour pressure of phosphorous remain higher than silicon vapour pressure beyond melting point of silicon. Phosphorous removing by evaporation from melted silicon bath would be easy under vacuum treatment. This process is also efficient to remove some metallic impurities as such aluminium, or silver which are expected impurities in Si scraps.

CEA has done such vacuum treatment of material coming from LOSER.

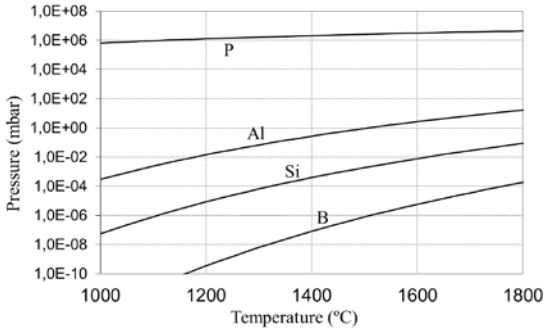


Figure 4: Vapour pressure of pure elements as function of temperature [6,7].

Experimental conditions and results are detailed in next paragraph.

3 ETCHING AND SOLIDIFICATION EXPERIMENTS WITH DISCUSSION

3.1 Directional solidification of lab scale ingots

A schematic of the furnace is shown in Figure 5. A typical charge size with poly-silicon is 12 kg, but since the charge tested here consisted of thin flakes, only 8.3 kg was possible to charge in the crucible.

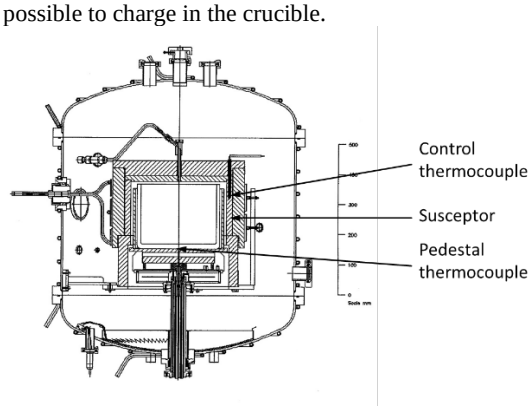


Figure 5: Schematic of the Crystalox DS-250 furnace at SINTEF.

The charge melted and solidified in a normal way except for shorter time for solidification than a standard charge due to lower ingot height.

After the ingot was produced, a central brick of 158mm*158mm was cut out for wafering by THM Fraunhofer in Freiberg, Germany. At the time of writing, the brick has been wafered, cell processing or characterisations will been done soon.

From one of the side cuts of the ingot, three samples were taken out and send for GDMS analysis at NTNU in Trondheim. The resulting measurements of boron, phosphorus and aluminium are shown in Table 2.

Table 2: GDMS measurements of B, Al, and P at three different (relative) heights in the ingot.

Height fraction	B (at/cm^3)	Al (at/cm^3)	P (at/cm^3)
0,28	1,80E+16	1,10E+15	1,59E+16
0,49	1,83E+16	1,13E+15	2,00E+16
0,87	2,45E+16	4,97E+15	5,74E+16

The concentration of P is higher than the sum of B+Al, indicating n-type material. It also shows that not all of the diffusion layers were removed.

The question was then: What went wrong?

The answer was found in the thickness measurements. New thickness measurements was done on the non-etched and large scale etched material from LOSER. 30 randomly picked samples were chosen from both batches. The resulting histograms (with fitted normal distributions) are shown in Figure 6 and Figure 7. These show that only between 5 and 10µm was removed from each side of the silicon flakes. This thickness reduction was too little in order to remove the ARC and both diffusion layers.

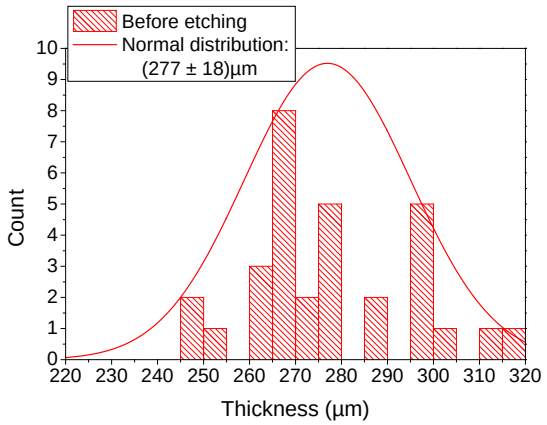


Figure 6: Thickness distribution histogram of 30 samples from the LOSER material before etching at SINTEF.

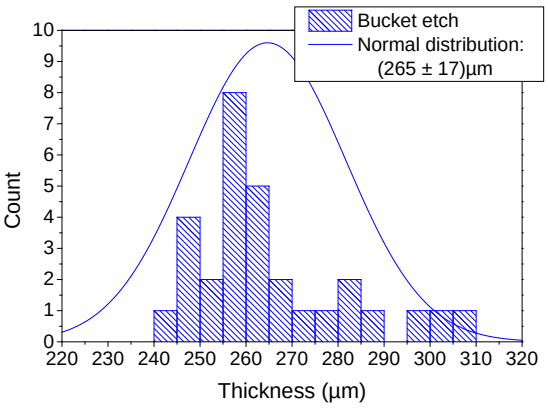


Figure 7: Thickness distribution histogram of 30 samples from the LOSER material after large scale etching at SINTEF.

After this it was decided to do more etching, but this time only small scale, and then rather do small scale directional solidification experiments with subsequent proper thickness and GDMS measurements.

3.2 New lab scale etching of LOSER and SOLITEK material

Three more etching batches were done at SINTEF. Again a "used polish etch" was used. One new batch of LOSER material and two batches of the SOLITEK material (taken after PECVD) was chosen. The thickness reduction is given by Figure 6 and 8 – 11.

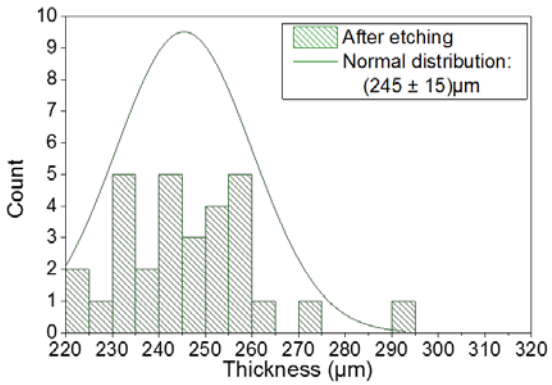


Figure 8: Thickness distribution histogram of 30 samples from the LOSER material after small scale etching at SINTEF. Thickness before etching is given in Figure 6.

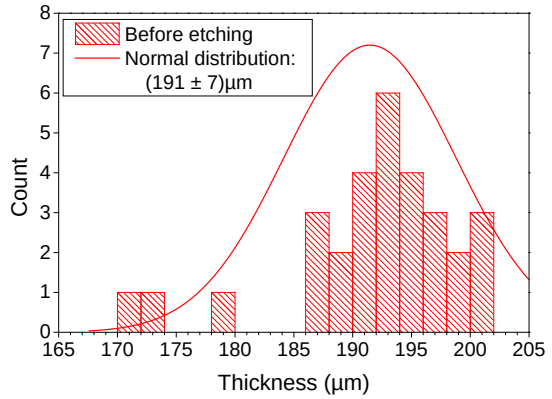


Figure 9: Thickness distribution histogram of 30 samples from the SOLITEK material before etching.

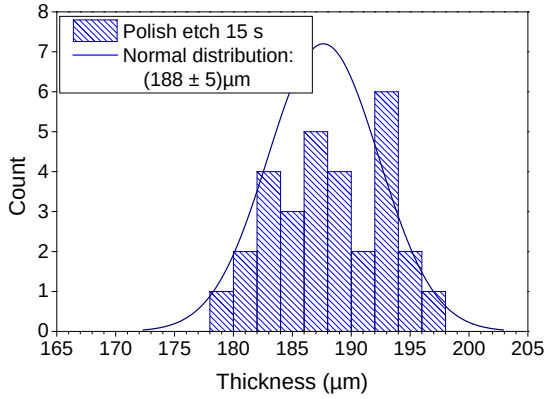


Figure 10: Thickness distribution histogram of 30 samples from the SOLITEK material after small scale etching in 15 seconds. Thickness before etching is given in Figure 9.

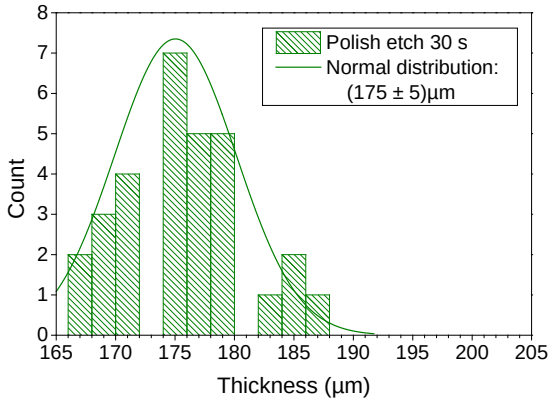


Figure 11: Thickness distribution histogram of 30 samples from the SOLITEK material after small scale etching in 30 seconds. Thickness before etching is given in Figure 9.

From the thickness distributions (Figures 6, 8 – 11), it is seen that the average thickness of the LOSER material has been reduced by about 16µm on both sides, and according to the Tof-SIMS measurements in Figure 2, this is sufficient for removal of the diffusion layer containing aluminium.

The two batches of SOLITEK material showed an average thickness reduction of about 1.5 and 8 µm on both sides. This should be enough to remove the Si_3N_4 ARC and P-diffusion layer.

3.3 Directional solidification test in small tube furnace

Directional solidification test in a tube furnace was performed at NTNU, Trondheim, Norway. A schematic of the tube furnace is shown in Figure 8. The furnace is designed as a traditional Bridgeman furnace, that is, the crucible with charge is slowly pulled down and out of the hot zone of the furnace leading to a controlled directional solidification of the metal. The sample size of the finished ingots are about 50 – 60 g, with a diameter of about 40 mm.

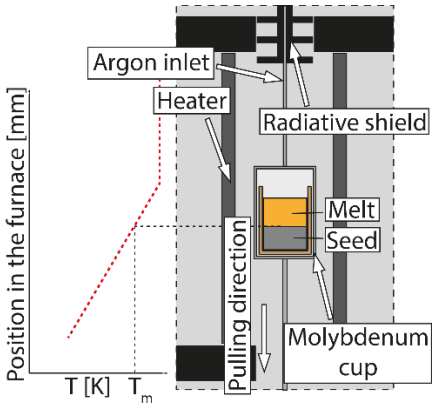


Figure 12: Bridgeman tube furnace at NTNU in Trondheim, Norway [8].

After the melting and crystallisation, two planes were cut from each samples and sent for GDMS analysis.

In total 6 different material samples were run in the small Bridgeman furnace. An overview of the different material is given in Table 3.

Table 3: Overview of the material tested in the small Bridgeman furnace.

Si-shards from LOSER	Wafers from SOLITEK
1. As received (with ARC, P, and Al)	1. As received (with ARC and P)
2. SINTEF etch	2. Etch 15 sec
3. Ferroatlantica etch	3. Etch 30 sec

The GDMS results from melting of the Si-shards from LOSER in the small Bridgeman furnace tests are shown in Table 4.

Table 4: Concentration of boron, aluminium, and phosphorus for the Si-shard samples (from LOSER) and the two heights. All concentrations are given in units of 10^{16} atoms/cm^3.

	Lower part			Upper part		
	B	Al	P	B	Al	P
As received	2.1	0.81	7.5	3.7	1.5	38
Ferroatlantica etched	2.3	0.49	0.16	3.0	1.1	0.38
SINTEF etched	1.6	0.17	2.0	2.9	0.71	6.1

For all the three small casts, there are higher concentration of the dopant elements in the upper region than in the lower one. This proves that the small ingots have been directional solidified.

The etching done at Ferroatlantica was more efficient than the etching done at SINTEF. Calculation of the net dopant level in the three ingots (B+Al-P) show that the ingots made from "As received" and "SINTEF etched" are n-type material whereas the ingot produced from the "Ferroatlantica etched" material is p-type. This concludes that even though about 16µm was removed from each side during etching at SINTEF, this was not enough. There is an uncertainty whether the sample analysed with Tof-SIMS (Figure 2) is representative.

The GDMS results from melting of the wafers from SOLITEK (containing only ARC and P-layer) are shown in Table 5. Since there were no aluminium diffusion layer in the SOLITEK-material, only boron and phosphorus were measured.

Table 5: Concentration of boron and phosphorus for the wafer samples (ARC and P layer containing wafers from SOLITEK) and the two heights. All concentrations are given in units of 10^{16} atoms/cm^3. The GDMS-signal for two of the samples had too much noise to be reliable.

	Lower part		Upper part	
	B	P	B	P
As received	0.66	3.5	0.73	6.6
Etched 15 sec	-	-	0.91	0.24
Etched 30 sec	-	-	1.0	0.10

The concentration of boron and phosphorus in the small ingots from the SOLITEK material shows that removing 1.5µm is enough to remove all the ARC and most of the P-diffused layer. For both ingots of the etched material, the material are p-type, whereas the ingot from the "As received" material is n-type.

A general comment for the small scale experiments is that larger scale testing must be performed in order to conclude regarding electronic properties of the material.

3.4 G2 ingot crystallisation from etched silicon

CEA produced one G2 ingot (55kg) by conventional directional solidification process using refined silicon from FAID etch process.

Picture of the ingot is shown in Figure 13. Applied recipes were standards one and no specific observations was done during the crystallisation.The ingot has been cut into two larges vertical cut of around 160mm thickness and observe by IR transmission imaging.

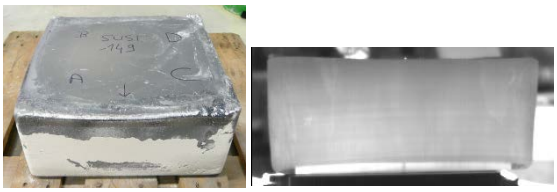


Figure 13: Picture of the ingot casting by directional crystallization done at CEA (at left) and IR transmission imaging.

The IR transparent image in Fig. 13 shows that no precipitates have been located.

The corresponding resistivity along the relative ingot height was measured using SEMILAB WT 2010D device. The resistivity remain low in the range of 0.4 to 0.6 Ω.cm indicating high dopant concentration.

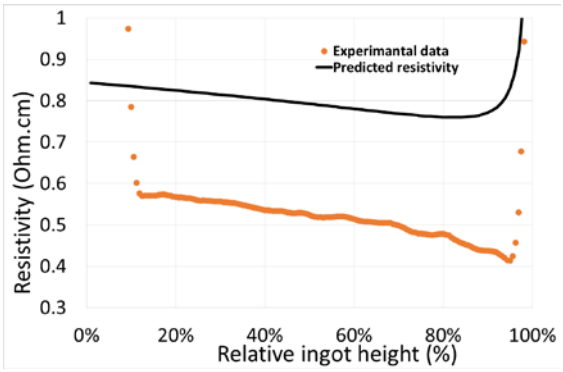


Figure 14: Resistivity profile of G2 ingot from etched silicon along relative ingot height.

4 PYROMETALLURGICAL REFINING AND SOLIDIFICATION EXPERIMENT

4.1 Vacuum treatment experiment

In this work, de-metallized broken silicon cells were

treated under vacuum refining condition. The silicon is introduced in a laboratory vacuum induction furnace. Crucible filling capacity is around 2-3kg depending material shape.

2.8kg of de-metallized broken silicon cells were melt in a graphite crucible. Experiment was done at temperature high above silicon melting temperature, under vacuum conditions and during a sufficient time to ensure high phosphorous content extraction. At the end of the treatment, the purified silicon is directly poured and quickly cooled in graphite mold. A purified silicon ingot of 2.46kg was obtained (Figure 16). Overall silicon mass yield is about 88%.

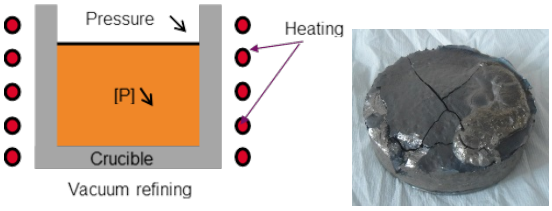


Figure 15: Schematic vacuum induction melting process (at left) and picture of the purified Si-ingot (2.46kg) (at right).

The concentration of the impurities was measured before and after refining respectively by ICP-OES (Inductively Couple plasma-Optical Emission Spectrometry) and GDMS (Glow Discharge Mass Spectrometry).
Samples have been directly taken for the silicon melt, assuring sample homogeneity. Chemical analysis results are given on the following table 5.

Table 6: Chemical analysis of de-metallized silicon broken cells before and after vacuum refining.

	before vacuum refining	after vacuum refining
elements	ICP-OES analysis Content (ppm wt)	GDMS analysis Content (ppm wt)
P	7.24	0.13
B	< 0.06	0.24
Al	29.02	0.16
Ag	125.23	0.14
Cu	0.43	< 0.01
Fe	0.36	2.3
Pb	1.30	< 0.005
Zn	0.28	< 0.01
Ti	0.90	0.17
Ni	< 0.32	0.38

Table 7: Light element concentration measurement before and after vacuum refining.

Light element analysis by IGA		
elements	Content (ppm wt) Before refining	Content (ppm wt) After refining
C	90	82
N	26	<1
O	29	4.7

The main impurities quantified in the de-metallized broken silicon cells are aluminum, phosphorous and silver. A small amount of lead was detected and few quantities of iron and titanium are present. Other impurities are in lower trace or under detection limit.

After refining, except for boron and iron, all impurities content are reduced. This reduction is particularly significant for P, Al and Ag. This demonstrates the efficiency of the vacuum refining process.

Light element concentration (C, O and N) were measured by IGA (Interstitial Gas Analysis). Low nitrogen content were measured. This proves that no pre-treatment to remove ARC layer is necessary. Oxygen contamination was widely reduced. Only carbon contamination remains in the matrix due to the use of graphite crucible.

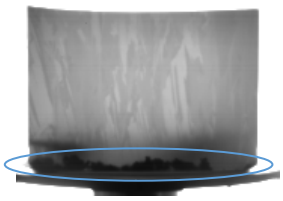
4.2 G1 ingot crystallisation from vacuum process

After refining, CEA used the purified silicon to produce one G1 ingot size by conventional DSS crystallization.

Blending of purified silicon with electronic grade silicon was performed to produce an ingot of 10kg. 2.4kg of purified silicon was mixed with 7.6kg of electronic grade silicon and loaded in a silica crucible. The overview of the ingot is shown in the Figure 17.

After lateral side cropping, the ingot was observed by IR transmission imaging to localized defects or precipitate into the silicon ingot as it can be seen on the Figure 17b. Some defects can be observed at the bottom part of the ingot as dark zones.

First optical microscopy observations reveals cavity-like defects. More investigation will be performed to understand the origin and the nature of those cavity-like defects.



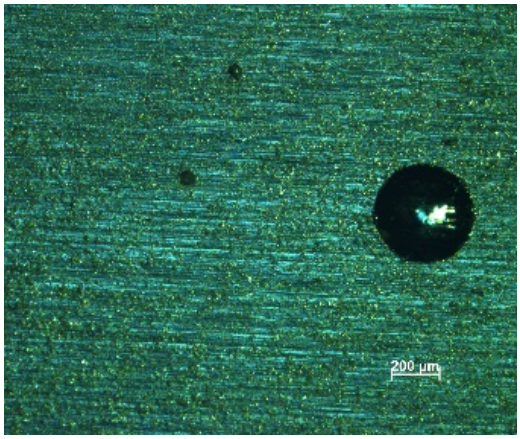


Figure 16: Silicon ingot picture (at left), IR transmission imaging of the ingot (at right) and optical microscopy imaging (c) of the dark bottom part (Fig 15.b) revealing cavity like defects.

Predicted resistivity without and with blending versus solidified fraction have been calculated from Arora mobility model regarding dopant concentration profile according to Scheil law.

Resistivity profiles along relative ingot height are plotted on Figure 18. Resistivity mapping was performed by SEMILAB WT 2010D.

The lower curve shows a simulation of the resistivity profile of the purified silicon without blending. This is one of a reason why blending has been suggested to achieve high resistivity compatible for solar cells processing.

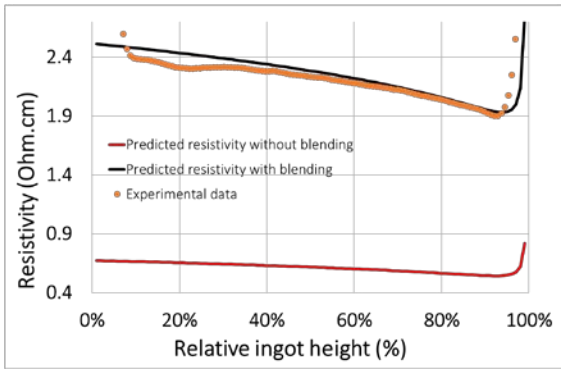


Figure 17 : Resistivity profile along relative ingot height (reporting data of middle of one lateral side). Comparison with predicted resistivity without and with blending with EG-Si.

Measured resistivity fitted well with the resistivity prediction with blending (top curve). Obtained resistivity are in the range 1.9 to 2.4 Ohm.cm and so in-spec with standard solar cells processing.

The next steps of the study will be to make wafers and cells from this ingot to test the material all along the production line. Processes and materials need more investigations to have a better control of final doping levels and limit the blending.

5 CONCLUSIONS

Based on the experiments done so far, the following conclusions can be drawn:

- Regarding the etching, "Used polish etch" or "9:1 etch" are suited for the etching of ARC and diffusion layers. A proper stirring of the mixture “etch – Si-shards” plays also an important role. And strong time vs. ΔT dependency has been observed.
- It has been shown that vacuum process is very efficient to remove ARC and diffusion layers for P-type waste (Phosphorous emitter layer can be easily removed by the vacuum treatment). It is also important to note that control of final doping level works better due to the homogeneous liquid state step.

Recycled silicon from the two routes have been crystallized using DSS process. Electrical and IR characterizations of ingots showed first good results. However more investigations are needed to understand cavity-like defect found on the ingot produced after the vacuum process.

Larger scale is needed for wafer production and testing of electronic properties to provide economical suitability of the different processes and routes.

Finally, the two process routes described in this paper will be transferred to solar cells coming from end-of-life modules.

6 ACKNOWLEDGEMENTS

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